Hybrid Additive Manufacturing of Embedded Electronics

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Abstract

Combining metal nanoparticle printing with polymer additive manufacturing has the potential to enable the manufacturing of devices with embedded electronic elements. State-of-the-art manufacturing processes offer a trade off between circuit resistivity or polymer damage. The goal of this work is to significantly decrease interconnect resistivity without damaging the substrate. In order to accomplish this goal we explore the mechanisms of Fused Filament Fabrication (FFF) of Acrylonitrile Butadiene Styrene (ABS), printing of silver NPs and out-of-chamber Intense Pulsed Light (IPL) sintering of the printed circuits. While attempting to achieve appropriate levels of circuit resistance, IPL of only-nanosphere based circuits lead to thermal damage of the polymer. However, a combination of both Ag nanospheres and nanowires achieves a resistivity several times lower than state-of-the-art (13.1 μΩ-cm or 8 x bulk silver) without any polymer damage. This circuit was sintered within 0.75 s of IPL

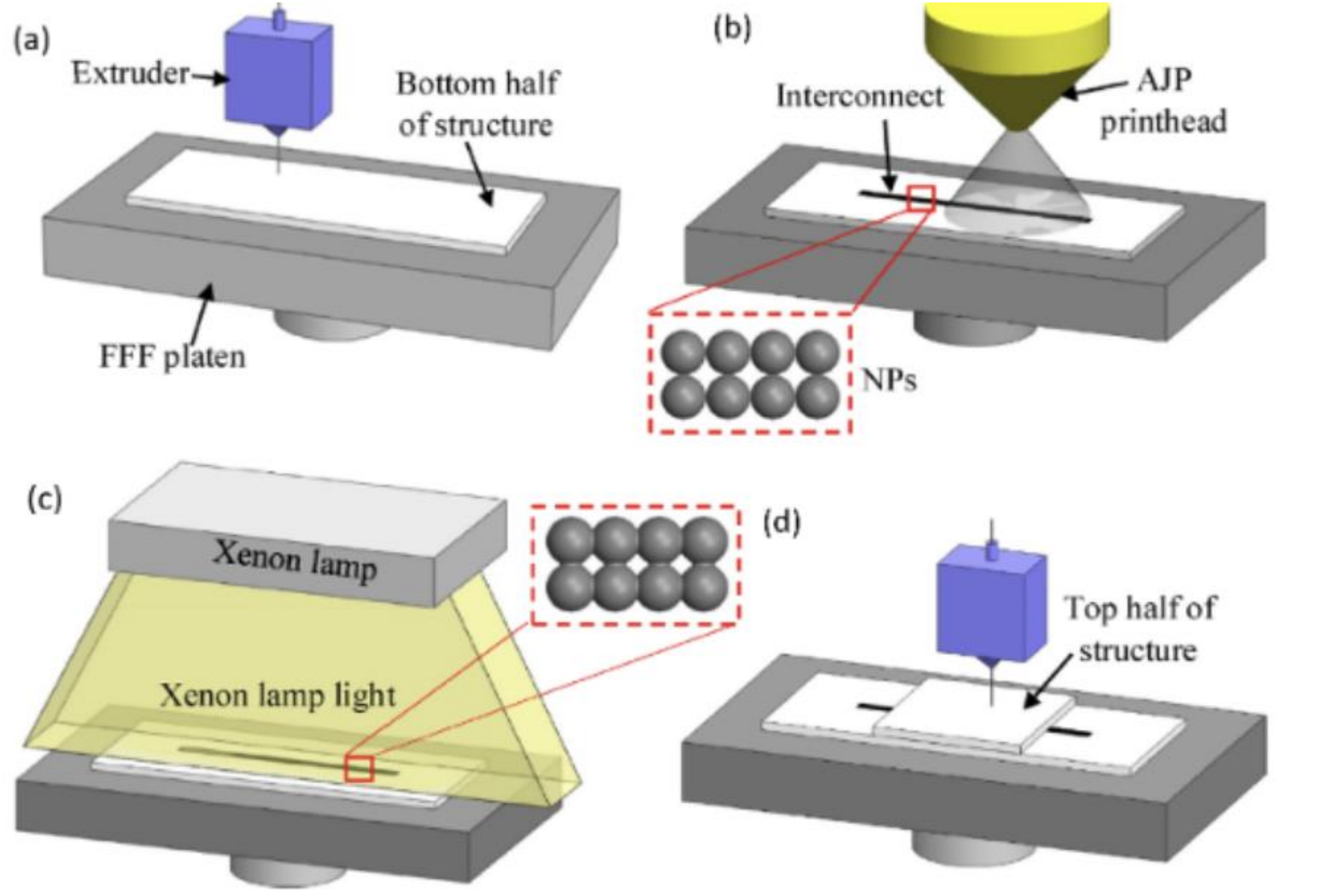

Fig.1: Schematic of Printing Process: (a) FFF of bottom structure (b) AJP of interconnect (c) IPL (d) Overprinting of top structure

Future Direction

The future goal of this project is to construct a novel, hybrid 3D printer capable of combining all the manufacturing processes into one. This would enable the uninterrupted manufacturing of embedded structures with 3D patterned interconnects. Creating this device would also serve as a testament to the scalability of the manufacturing process as well as a significant increase in throughput capability.

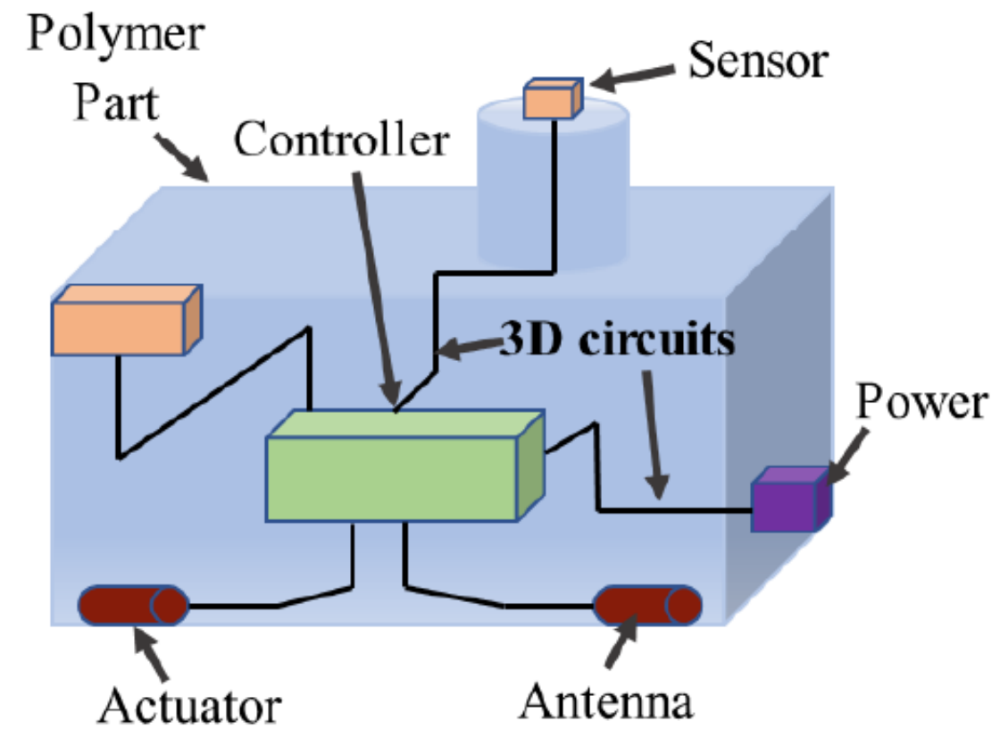

Fig. 6: 3D Embedded Electronic

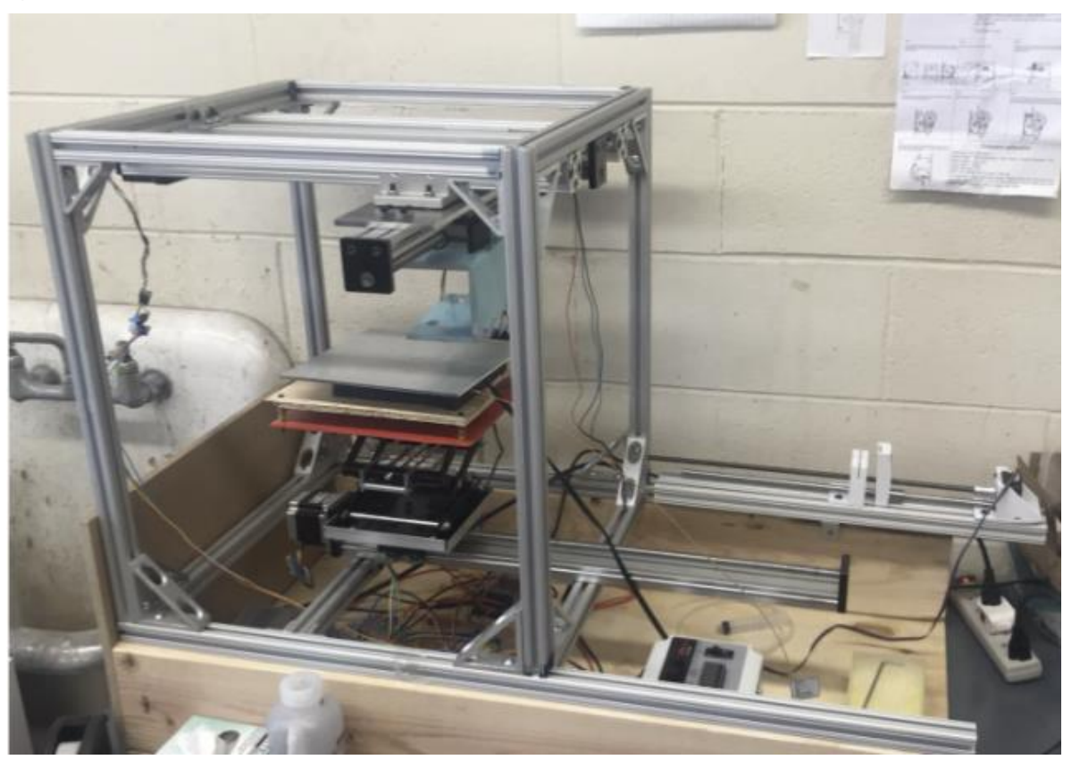

Fig. 7: Hybrid 3D Printer in Construction

Experimental

The polymer substrate base was fabricated using a CraftBot Plus FFF printer (Craftunique), the build plate was then removed form the printer and the Ag NP ink was then deposited onto the substrate via an Aerosol Jet Printing (AJP) head with the use of laser-cut polypropylene masks, the build plate is then moved to the IPL Sinteron 3000 system (Xenon Corporation) where the silver NP's are sintered together. The build plate is then moved back to the Craftbot printer where additional material is deposited on top of the printed circuit(Fig. 1). Lengths of copper tape are attached to the ends of the deposited circuit to measure electrical resistance values.

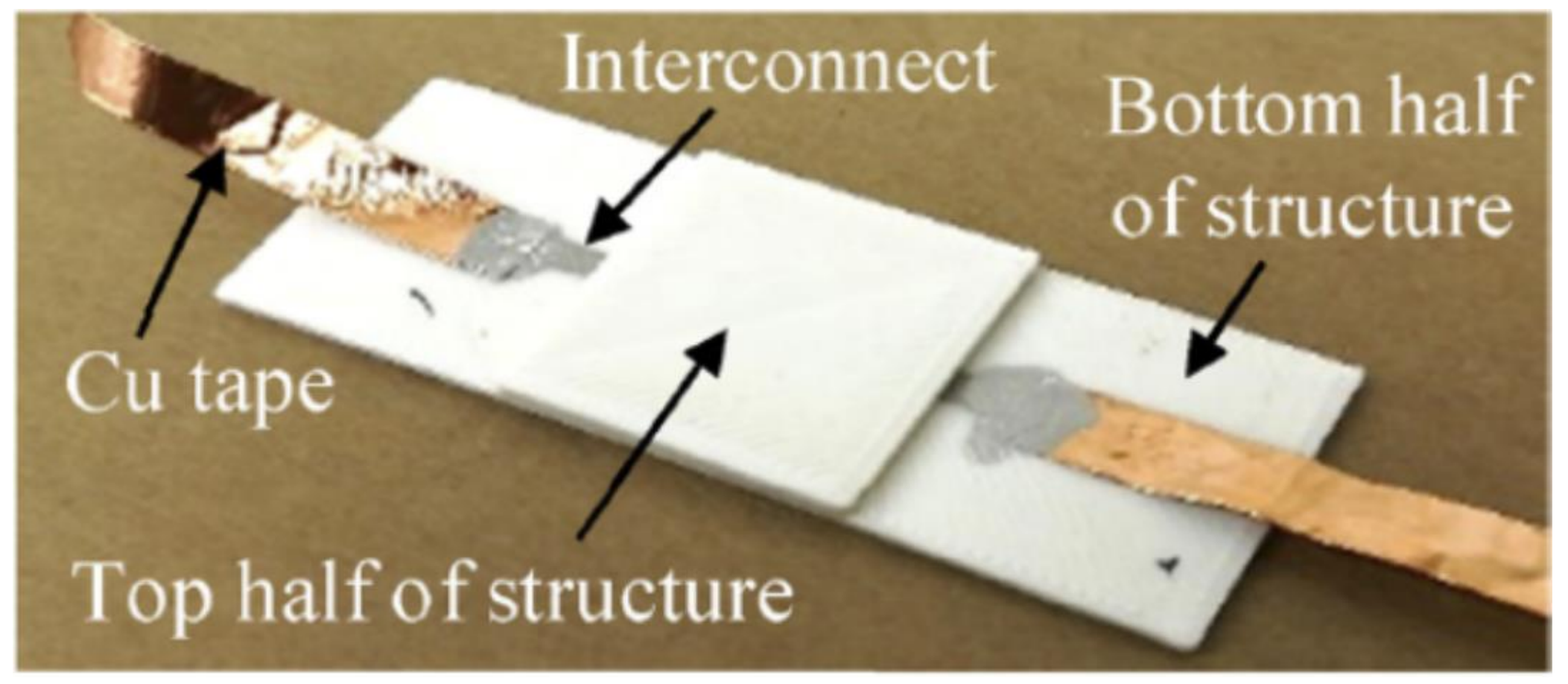

Fig. 2: Completed Sample with Embedded Circuit

IPL parameters for sintering of the deposited inks were varied to achieve the lowest resistance possible, changing both fluence J/cm^2 and number of pulses applied. Increasing the fluence or the number of pulses would cause a reduction in resistance up until a certain point after which IPL damages or evaporates a portion of the circuit causing a spike in resistance. In addition to changing IPL parameters, ink formulae were changed to find the optimal NW:NS combination for the lowest resistance possible.

Results and Discussion

The highest as-printed resistances were seen with interconnects that had a NW:NS ratio of 0:100, this resistance was on the order of MΩ. When attempting to find optimal IPL parameters for the 0:100 NW:NS ratio the ABS substrate is significantly damaged before any appreciable reduction in resistivity is observed.

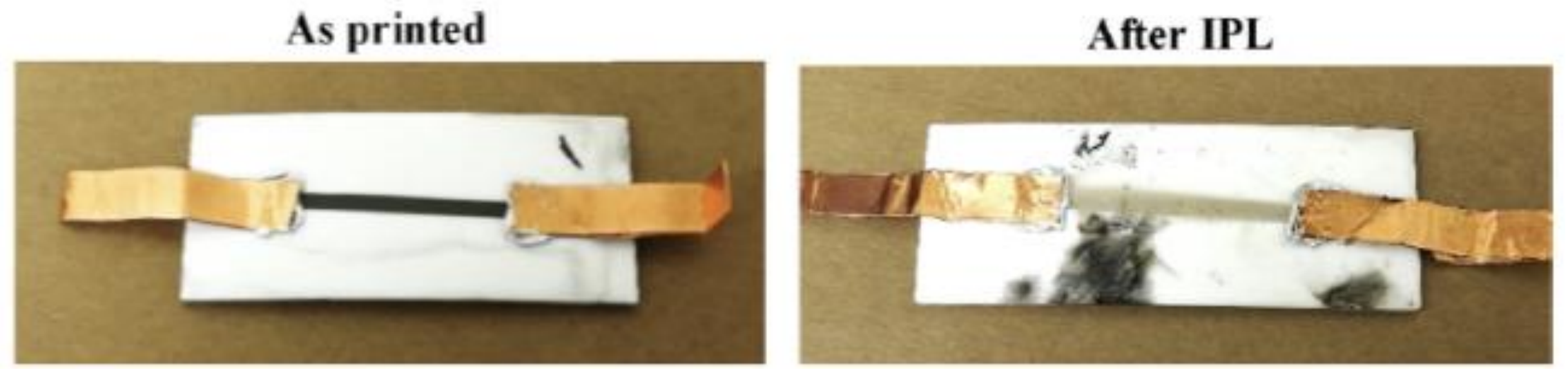

Fig. 3: Damage on ABS substrate with 0:100 NW:NS Ratio Interconnect

Interconnects comprised of both NW and NS had significantly lower as-printed resistances, and had notable decreases in resistance without any damage occurring on ABS substrate. As-printed resistivity decreases with increasing NW content, lowest as-printed resistivity is seen with 100:0 NW:NS(22 μΩ-cm). Additionally, interconnects with greater NW content also see greater reductions in post-IPL resistivity, the lowest value achieved was 13.1 μΩ-cm for a NW:NS ratio of 100:0. This resistivity is 3.8 times lower than state-of-the-art damage-free oven annealing.

Table 1: Optimal Fluence and Pulses for various NW:NS Ratios

NW: NS	Fluence (J/cm^2)	No. of pulses	Total time (s)
25:75	2.5	3	1.3
50:50	3	3	1.5
100:0	4.5	1	0.75

Dynamic changes in resistivity were measured during the over printing process (Fig 4). The vertical lines of the graph indicate the completion of an ABS layer deposition (layers 1–6).

Dynamic changes in resistivity were measured during the over printing process (Fig 4). The vertical lines of the graph indicate the completion of an ABS layer deposition (layers 1–6). Initially there is a minor reduction of resistivity in stage A. After about 25% of the first layer is deposited there is a more significant increase in resistivity which lasts until the completion of layer 1 deposition. In stage C, deposition of layers 2 through 4, the resistivity remains constant or decreases slightly. In stage D, deposition of the 5th layer, there is a sharp decrease in resistivity. After deposition of layer 5 there were no further reductions in resistivity, even after printing a 6th layer.

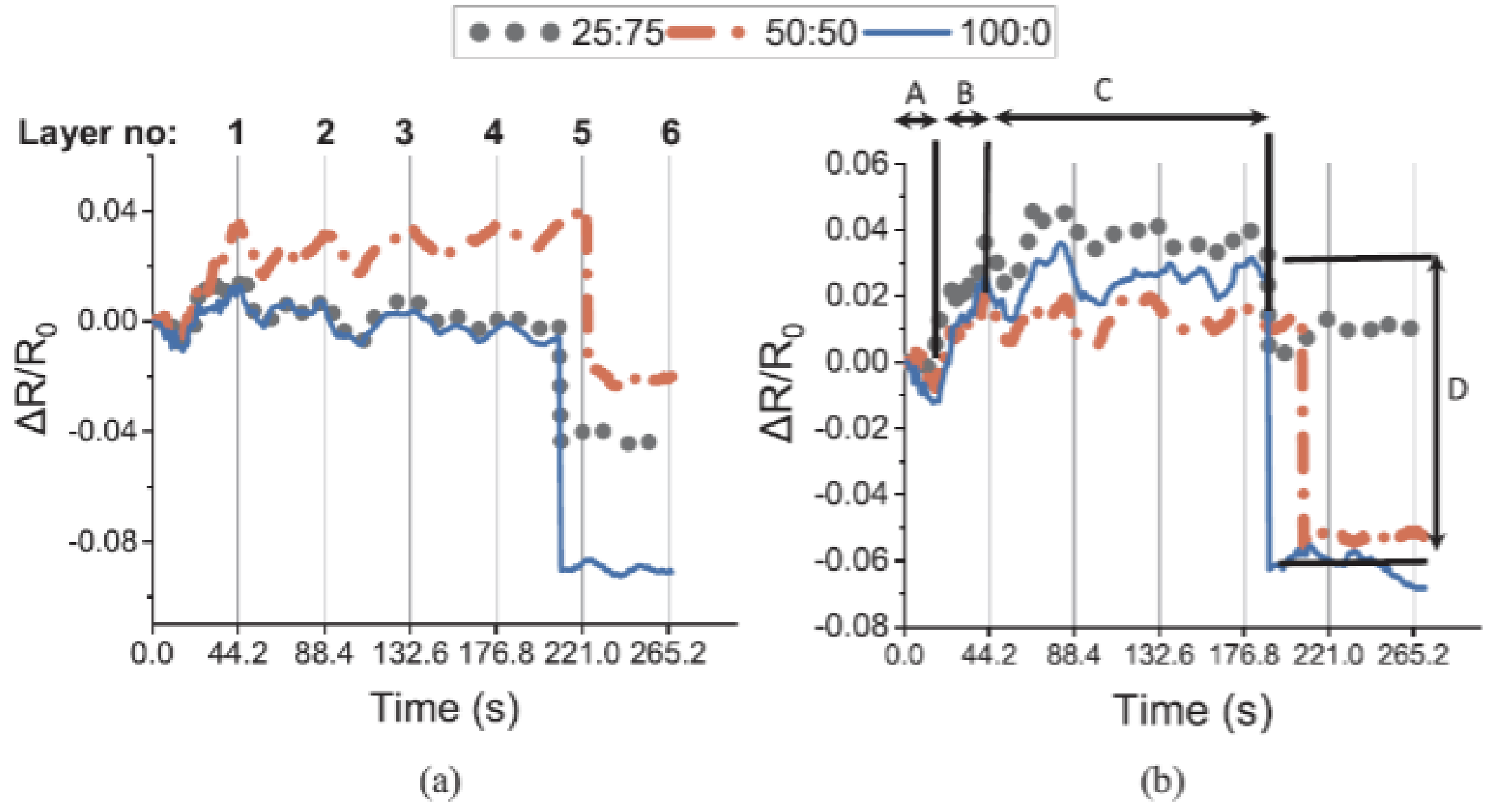

Fig 5. Dynamic resistivity during overprinting (a) unsintered samples (b) post-IPL samples.

The following mechanisms are responsible for the observed resistivity changes during overprinting. First is the temperature-induced increase in resistivity of metals due to heat transfer from deposited polymer. Second is thermomechanical stress, the tensile stress during expansion can break interparticle necks and increase resistivity and compressive stress during shrinkage can increase interparticle neck size to reduce resistivity. Final mechanism is the temperature-induced sintering which can reduce the resistivity during overprinting.

Acknowledgements

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